



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/642,458	08/18/2000	Alexander G. MacInnis	37259/SAH/B600	7111

23363 7590 02/11/2004

CHRISTIE, PARKER & HALE, LLP  
350 WEST COLORADO BOULEVARD  
SUITE 500  
PASADENA, CA 91105

EXAMINER

HAVAN, THU THAO

ART UNIT	PAPER NUMBER
----------	--------------

2672

28

DATE MAILED: 02/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/642,458

Applicant(s)

MACINNIS ET AL.

Examiner

Thu-Thao Havan

Art Unit

2672

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 19 November 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-3, 5-39, 41, 42, 46 and 48-51 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-39, 41-42, 46, and 48-51 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 27.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments with respect to claims 1-3, 5-39, 41-42, 46, and 48-51 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims **1-3, 5-39, 41-42, 46, and 48-51** are rejected under 35 U.S.C. 102(e) as being unpatentable by Sporer et al. (US patent no. 5,883,670).

Re claim **1**, Sporer teaches a system on an integrated circuit chip comprising an MPEG video decoder for processing MPEG video data to generate video for displaying and means for displaying the video (col. 10, lines 1-29; figs. 1 and 9), a system bridge controller for coupling a CPU to a plurality of peripheral devices (figs. 1 and 3), wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip (col.3, line 54 to col. 4, line 28), and wherein the system bridge controller supports delayed read and retry of reads by external masters (col. 8, lines 46-56). In other words, Sporer teaches a digital motion video processing circuit can capture full-

rate motion video information and playback full-rate motion video. Motion video information may also be manipulated to perform effects. The video processing circuit uses the system memory of a computer as a data buffer for holding compressed video data from the circuit. The system memory may be accessed by the circuit over a standard bus. A controller in the circuit directs data flow to and from either the standard bus or the input/output port through processing circuitry for compression, decompression, scaling and buffering. The standard bus may be a peripheral component interconnect (PCI) bus. In addition, the interface includes a read buffer, implemented as a first-in, first-out (FIFO) memory and a write buffer, also implemented as a FIFO, along with control and configuration registers. The master interface also has two direct memory access (DMA) channels. One DMA channel is used to transfer information from the PCI bus to the generic bus interface. The other channel is used to transfer information from the generic bus interface to the PCI bus. The master interface generally is used to transfer pixel data. The PCI interface, under most conditions, performs a READ Line or Write Line burst mode transfer to optimize performance on the PCI bus.

Re claims **2-3, 14, 18-19, 23, 25, and 49**, Sporer discloses the system bridge controller is capable of performing format conversion between big-endian data and little endian data, between the CPU and one or more of the plurality of peripheral devices, between the CPU and at least one of the MPEG video decoder, the means for displaying the video and the other components for processing video and graphics (figs. 1-3).

Art Unit: 2672

Re claims **5 and 26**, Sporer discloses plurality of peripheral devices include one or more PCI devices and wherein the system bridge controller includes a PCI bridge for coupling the CPU to the one or more PCI devices (col. 7, line 58 to col. 8, line 41). In other words, Sporer teaches the PCI interface implements a standard PCI configuration space and is used for all communication between a host computer system and for all memory transfers between the video processing circuit and the system memory. Dual address cycle and special cycle modes may be unsupported. The PCI interface enables the video processing circuit to act as a slave device (target) or as a full bus master to move data between system main memory and the video processing circuit.

Re claims **6, 10, 27, and 31**, Sporer discloses the PCI bridge is capable of performing a DMA function between the one or more PCI devices and an external memory (col. 8, lines 22-45; col. 11, line 1 to col. 12, line 22).

Re claims **7-8 12-13, 28-29, 33-34, and 37-38**, Sporer discloses PCI bridge is capable of performing format conversion between big/little endian data used in the CPU and little/big endian data used in the one or more PCI devices (col. 1, line 52 to col. 2, line 9; col. 7, line 58 to col. 10, line 67).

Re claims **9, 30, and 50-51**, Sporer discloses plurality of peripheral devices include one or more I/O devices, and wherein the system bridge controller includes an I/O bus bridge for coupling the CPU to the one or more I/O devices (fig. 1—elements 37 and 39; col. 4, lines 10-28).

Re claims **11 and 32**, Sporer discloses one or more I/O devices include a device selected from a group consisting of ROM, RAM, flash memory and 6800-compatible peripheral devices (col. 6, lines 36-54; col. 9, lines 32-67; fig. 5).

Re claims **16 and 35**, Sporer discloses CPU interface block is capable of performing burst accesses of the CPU in both read and write directions (col. 9, lines 55-67; col. 4, line 64 to col. 5, line 33). Sporer teaches a memory system includes a computer readable and writable operation.

Re claims **17 and 36**, Sporer discloses CPU interface block includes one or more buffers used to resolve a speed difference between the CPU and external SRAM devices (col. 5, lines 15 to col. 6, line 15). Sporer teaches the processor causes data to be read from the non-volatile recording medium into an integrated circuit memory element, which is typically a volatile random access memory, such as a dynamic random access memory (DRAM) or static memory (SRAM).

Re claims **22 and 41**, the limitations of claims 22 and 41 are analyzed as discussed with respect to claim 1 except for the integrated circuit chip is used to process MPEG video data to generate video for displaying and to display the video; and an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data, an MPEG video decoder for processing the MPEG video data to generate video for displaying. However, Sporer teaches the claimed limitations when he discloses decoding MPEG format video (col. 6, lines 1-55; col. 10, lines 1-29). In that he discloses an MPEG interface connects to the MPEG codec. A DRAM controller controls the DRAM buffer

Art Unit: 2672

used by the MPEG codec. A JPEG interface is provided for controlling the raster block converter and JPEG codec. A PCI interface is used to connect to the PCI bus. A generic bus interface (GBIF) is implemented to control access to the generic bus by the PCI configuration EPROM, MPEG decoder, JPEG codec and video encoder and to provide a data path that is used to transfer data to/from the JPEG and MPEG codecs, including the transfer of pixel data during various effect rendering modes.

Re claims **15, 20-21, 24, 39, 42, 46, and 48**, the limitations of claims 15, 20-21, 24, 39, 42, 46, and 48 are analyzed as discussed with respect to claims 1, 22, and 41 above.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Walsh et al., US patent no. 5,903,261

Mino et al., US patent no. 6,077,084

Foster et al., US patent no. 6,662,329

### ***Inquiries***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thu-Thao Havan whose telephone number is (703) 308-7062. The examiner can normally be reached on Monday to Thursday from 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on (703) 305-4713.

Application/Control Number: 09/642,458  
Art Unit: 2672

Page 7

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231


or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Thu-Thao Havan  
February 6, 2004



MICHAEL RAZAVI  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600